DIRECT BOND COPPER (DBC) TECHNOLOGIES

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INTRODUCTION

Direct Bond Copper technology that primarily uses copper foil bonded directly to ceramic substrates was originally developed and patented by General Electric Company in the early 1970's and subsequently protected with a series of other patents. Although jewelry makers in fabrication of copper costume jewelry for many years have practiced a similar process, GE was able to patent the technology for its application to ceramics. The technology, which required royalty licensing, offers advantages over traditional thick and thin film metalization technologies for a wide range of modern microelectronic applications. The inherent advantages of using bulk metal copper foil in place of fritted or reactively bonded pastes and economically expensive sputtered metalizations is increasingly finding wide ranging applications across the span of military, commercial, industrial, and automotive industries as engineers readily accept the electrical and thermal properties of a traditionally favorite copper system for electronic circuits. The standard Direct Bond Copper or DBC technology which uses copper foil thicknesses in the range of 0.005 to 0.020 inches is usually specified for high power and high thermal management circuits where the large geometry requirements of 0.015 inch wide lines and spacings can be used. New processes and additional refinements of the process which adapt the inherent advantages of the strong bonding mechanism of the DBC process however, will allow the technology to be adapted for fine line circuitry and will extend its applications to high frequency circuits.

DBC PROCESS

The DBC process uses OFHC (oxygen free) or ETP (tough pitch) copper foil which has been oxidized by chemical or thermal means to provide a uniform dark blue-gray CuO cupric oxide coating thickness, on the copper surface. This foil is placed on the face of an oxide ceramic such as alumina or beryllium oxide and introduced through an inert tunnel furnace, which is usually continually purged with nitrogen. >From the phase diagram reproduced from an early GE patent 3,994,430 (Figure 1), it is evident that a liquidus region at 1 .54 atomic percent oxygen exists at 1065 °C**.** The belt furnace is profiled in a high peaked bell shape thermal distribution to bring the copper and ceramic to a temperature above the 1065 °C eutectic bonding temperature at which the copper oxide forms a liquidus cuprous oxide (Cu_20) matrix which wets and chemically bonds to the oxide surface of the ceramic. Since the eutectic temperature is 18 °C below the 1084°C melting point of pure copper, the furnace profile must be tightly controlled to overcome loading- effects from both- the mass of the entering substrates and the cooling effects of the nitrogen gases. The resultant bond is highly tenacious and rugged. With alumina and beryllium oxide surfaces bond strengths exceeding 24,000 PSI are readily achieved. The conversion of the initial cupric oxide (CuO) formed on the copper and the resulting cuprous oxide (Cu_20) - copper bond releases excess gas during the process which must be dissipated from the copper - ceramic interface to avoid gaseous entrapments under the copper which appear as blisters. These blisters which are normally referred to as *tents* to distinguish them from reliability problems associated with thin film blistering and plating blistering, are a commonplace phenomena and is one of the highest yield point losses in the process. This problem is also compounded as the area of the bonded surface increases to the large alumina Herman (3.75” x 4.5”) and super Herman (4.5” x 4.5”) sizes. To overcome this problem, the majority of DBC processes use copper foil that has been pre-etched on one side with a pattern of evenly spaced parallel grooves which when placed against the ceramic allow the dissipation of the gas during the eutectic formation preventing gas entrapment until the grooves become filled with eutectic themselves. Different vendors vary groove patterns and depths to optimize this technique for their oxidization process. These grooves although solving one problem leads to other subsequent process problems such as chemical entrapment during chemical etching, cleaning, or soldering processes; ceramic staining due to chemical entrapment during soldering or heat baking and; severe undercutting for fine line circuit patterns. They can also become a source for moisture entrapment during environmental screening which can lead to a rupture of the copper to ceramic bond during temperature cycling and thermal shock conditions. More modern techniques allow control of the oxide thickness to eliminate the grooves from the copper foil completely too totally eliminate these, problems. After the bond is formed the copper and ceramic is slowly cooled in the furnace to temper the copper foil to a dead-soft annealed condition and to control the copper grain formation. Excess oxygen and high temperatures can lead to a roughened alligator type skin condition due to high eutectic oxide segregating at the copper grain boundaries. This condition can result in an uneven surface texture and extensive nodule formation, which may disturb chip attachment and wire bonding. The annealing of the copper during its cool down phase is important to overcome the severe thermal expansion

mismatches of the copper and ceramic. Once bonded at DBC temperatures above 1065 °C, the large temperature differential to room temperature can lead to severe bowing and camber of the ceramic as the copper contracts at a faster rate. Proper selection of copper foil thickness to ceramic thickness with single or double sided bonding is important to match the thermal expansion coefficients and flexural strengths of the materials shown in Table 1 and Figure 2. Since there is an effective zero yield point for ceramic materials, improper selection - can result in ceramic fracture during temperature and thermal cycling.

To review, the DBC process yields exceptionally high strength bonds in excess of 24,000 PSI using copper foil with the bulk electrical and thermal properties of bulk copper and is bonded at an extremely high temperature, which permits substrates to be brought easily to Cu-Si and other high brazing temperatures without impairment to the bond. The rugged bond allows extensive rework to solder joints and wire bonds.

PATTERNED SUBSTRATES:

The bulk of the DBC substrates manufactured are small single chip versions used to mount power transistors and rectifiers and are typically less than 0.5" square. These substrates are economically manufactured using the price advantage of small pressed BeO substrates in a one-up configuration where operators manually line pre-etched -squares of copper on the ceramic substrates which **a**re placed on carrie**r'** bricks and sent through the bonding furnace. High volume applications allow automated pick and place machines to eliminate the tedium and misalignment problems associated with operator assembly. More sophisticated geometries require chemically milled copper that is either pre-etched and then bonded to the substrate, or is subsequently chemically milled after a full sheet of copper is bonded. The first approach requires copper bridges to hold the isolated islands of copper together for the bonding process, which must later be removed, and can also lead to distortions due to the large expansion rate of the copper. This approach also allows bonding of extended metalization for flying leads off the ceramic surface. The latter approach allows devices to be manufactured as multiple devices and a single substrate using batch orientated printed circuit board techniques for photopatterning. Typically dry film photoresist is applied to both sides of a copper clad substrate and standard photolithography processes are used to develop the circuit pattern into the photoresist. Certain design rules are required to be incorporated into the emulsion masks used in the process to allow for proper etch factors dependent on the thickness of the copper foil used and to allow space for a dicing grid to permit later separation of the individual substrates with either a diamond dicing saw or laser techniques. Front to back alignment masks in a clamshell orientation are required for double sided boards to permit a free copper area necessary for the diamond saw and laser techniques. Standard Autocad Gerber and DXF magnetic files are readily accommodated and are usually modified at the factory to add the details of etch factor, dicing grid, and alignment reticles. 24 Hour Bulletin board modem service is frequently provided to permit rapid development of prototype circuits.

PLATING:

Although DBC substrates can be used directly in microelectronic applications without plating using aluminum wire bonding directly to the copper foil, many applications require nickel or nickel and gold plating. Copper foil which comes directly from the DBC furnace is typically passivated with a thin oxide coating protecting itself from rapid deterioration by room temperature oxidation. Parts are frequently shipped in this state and are protected in packaging with moisture desiccants to prevent excessive oxidation. Nitrogen storage or storage in desiccant cabinets is usually recommended to further protect the circuits. Surface preparation used in photolithography can reduce this surface protection and parts are often protected with organic surface treatments. Plating of copper with nickel and gold can readily be achieved with electrolytic plating techniques where isolated island of copper areas can be electrically connected. For complex circuits with many isolated islands, specialized electroless nickel and gold plating techniques are adopted. Typical thicknesses specified are 50 -150 micro inches of nickel and 10 micro inches nominal of gold flash. Specialized and proprietary processes are required for gold thickness that exceeds 10 micro inches.

ELECTRICAL PROPERTIES:

The electrical properties of the DBC substrate assume the bulk characteristics of copper. Electrical resistivities of 2.5 micro ohm-cm permit high current loading. 12 mil copper foil with 0.040” line widths are capable of handling 100 amp continuous dc operations with low temperature increases of less than 20 °C**.** Another important advantage of the high conductance of the copper film is its reduction in resistive or IR loading terms in the Vce(sat) conditions of power transistors. This reduction on Vce(sat) conditions can allow increased drive currents and reduce transient switching times.

THERMAL PROPERTIES:

The addition of bulk copper foil to both the top and bottom of the ceramic can rapidly reduce the thermal resistance and thereby reduce the temperature rise of the junction temperature of the semiconductor chip. Users have reported doubling the thermal conductance as well as electrical conductance by substitution of DBC heat spreaders in place of thick film and refractory metalized ceramics. The reduction of junction operating temperature for semiconductors has a dramatic improvement in operating reliability and increases MTBF in Mil-Hdbk-217B calculations. This reduction also allows the designer to increase circuit densities and miniaturize the circuit elements. The copper foil has a dramatic effect on the effective thermal conductivity of the combination foil and ceramic. The copper foil assists in laterally spreading the heat along the surface of the substrate as well as increasing the spreading angle through the substrate. From **a.** conduction model reported in ISHM monograph 6984-003 entitled *Circuit Board Material/Construction and its Effect on Thermal Conductivity* by Mr. Guy W. Wagner the effective conductivity of a composite substrate can be calculated by the equation:

$$K_e = \frac{K_1t_1 + K_2t_2 + \ldots K_nT_n}{t_1 + t_2 + \ldots t_n}$$

where K = thermal conductivity of each material

t = thickness of each material

The thermal conductivities of common microelectronic materials are listed in Table 2. The effective thermal conductivity of cladding copper foil of differing thicknesses onto differing ceramic thicknesses is calculated in Table 3. As is evident in this table large improvements can be made by the excellent thermal properties of the copper foil. Whereas the ratio of thermal conductivities of alumina to beryllia is over ten times for the raw material, the influence of the copper cladding process will narrow this gap near a two to one ratio. Many applications can substitute economical alumina for the more expensive BeO. Designers who have learned to economize by minimizing metal areas in thick and thin film circuits to reduce, precious metal costs can increase thermal performance by only removing copper foil where electrically necessary. This technique gives DBC its distinctive appearance in circuit designs with its massive areas over the sparsely designed traditional circuitry.

Another effect associated with the copper cladding is its low transient thermal response. Due to mass and high thermal capacity of the copper foil~ semiconductors can be run at high peak pulses and short surge currents with a slow response in thermal heating effects.

MECHANICAL PROPERTIES

The general mechanical properties of ceramics and DBC substrates are listed in Table 4 and Table 5 respectively. The tenacious bonding of the copper foil to ceramic allows repeated rework to soldered connections and to wire bonding applications. Unlike the fragility of thick and thin film circuits, the DBC circuits allow rough handling and can endure repeated eutectic bonding temperatures. The selection of the ratio of copper thickness to ceramic thickness is an important consideration in the initial design of the circuit. One-sided bonding on thin substrates can cause severe camber conditions that can degrade the bond with repeated temperature cycling due to shear and *bimetallic* type bending forces or lead to ceramic fracturing. These effects can be reduced by double sided bonding to equalize the forces between opposite faces of the ceramic. Leaving copper in non-electrical areas will not only improve lateral heat spreading but also minimize bending stresses during temperature cycling. Since excessive camber can lead to solder voiding during substrate attachment and subsequent degradation of thermal performance due to air entrapment, the ceramic is often designed to be thicker than a traditional thick or thin film circuit. With the improved thermal performance of the copper, this increase in dielectric thickness can minimize cambering leading to improve substrate attachment and less bending stresses on the copper foil.

FUTURE DEVELOPMENTS

The exceptional bonding strength and high reliability of the DBC process combined with the electrical and thermal performance of copper conductor circuitry has taken DBC from early prototypes to production quantities for high power, high current, and high temperature applications. New DBC related processes are continually being developed to meet the challenges of other technologies. A few of these applications include:

POWER PACKAGING:

Special hermetic copper power feedthru techniques are being tested to permit high current applications with low IR conductance losses. Power feedthrus capable of handling over 100 amps with less than 100 micro-ohm resistances are being designed.

POWER RESISTORS:

The DBC techniques are not limited to copper oxide eutectics but can work with other metallic oxides. Special bulk alloy foils used as resistor elements are being eutectic alloy bonded directly to ceramics to take advantage of the exceptional power handling capabilities of the process and to incorporate power RF terminations.

MICROWAVE:

The thickness of the copper foil however limits fine line geometries and repeatable etching resolutions for high frequency applications and large digital circuitry. New developments in prototype development permit a combination of DBC and pattern plate-up techniques using printed circuit board technologies of acid copper plating to offer products to span the microwave and digital fields.

NON OXIDE CERAMIC BONDING:

Special processes are required to bond other non-oxide ceramics. Aluminum nitride which offers an attractive alternative to the inherent economic and environmental disadvantages of beryllium oxide requires specialized surface oxidation to permit DBC bonding. Most thermally grown oxides on AIN result in a bauxite alumina coating that is porous and weakly adherent to the underlying AIN surface. Not only is this interface a poor thermal conductor between the copper and AIN materials but it is also mismatched in thermal expansion characteristics between the materials. The high stresses induced by the mismatch with copper in the high bonding temperatures of the process as well as the reduction effects' of the inert atmosphere of the nitrogen gas used in the process result in a stressed interface. Repeated temperature cycling and thermal shock can easily rupture this interface with loss of adhesion occurring at the alumina to aluminum nitride interface. Specialized techniques to achieve a graded and highly dense but thin interface are required to optimize the bonding between the AIN and its oxide surface.

CONCLUSIONS:

Direct Bond Copper (DBC) Technology from its' earlier applications in appliance modules and refrigeration controls finds increasing usage in high technology hybrid power applications. From advanced radar systems and submarine sonar circuitry to industrial power control and automotive applications, DBC is capable of handling the extremely high electrical current and high thermal cooling requirements that cannot be done with conventional thin and thick film metalization technologies. DBC has developed alongside with recent advances in power semiconductors that eliminate the old power tube devices to supply the hybrid designer with a cost effective microelectronic and packaging technology. Applications for high current, high voltage, high power, and high temperatures can all be accommodated by a low cost, reworkable metalized substrate material that will become the standard in the next generation of electronics.

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TABLE 1
THERMAL EXPANSION & FLEXURAL STRENGTHS

Material	Thermal Expansion Coefficient	Flexural Strength
Alumina (96%)	6.3 - 7.4 x 10^{-6}/°C	420 mPa
Alumina (99.5%)	6.7 - 7.1 x 10^{-6}/°C	360 mPa
Beryllium Oxide (99.5%)	8.47 x 10^{-6}/°C	230 mPa
Beryllium Oxide (Zirconia doped)	7.6 x 10^{-6}/°C	350 mPa
Aluminum Nitride	4.6x 10^{-6}/°C	350 mPa
Copper (99.9%)	17.8x 10^{-6}/°C	
Gallium Arsenide		
Silicon	4.0x 10^{-6}/°C	
Kovar	21.4x 10^{-6}/°C	
Cu-Sil Braze	18.5 x 10^{-6}/°C	
In-Cu-Sil Braze	18.2 x 10^{-6}/°C	

TABLE 2

THERMAL CONDUCTIVITIES

Material	Thermal Conductivity (W/mK) 25°C	150°C	200 °C
Alumina (96%)	20	15 ‘	.
Alumina (99.5%)	34	25	
Beryllium Oxide (99.5%)	260	181	151
Beryllium Oxide (Zirconia doped)	240	162	139
Copper	386		
Gold	314		
Silicon	125		
Kovar	17		
Solder (60/40)	49		
Air	0.03		

TABLE 3

THERMAL RESISTANCE CALCULATIONS*

Material	Thickness	Copper Thickness	Equivalent Thermal Conductivity (W/mK)	
			One Side Copper	Two Side Copper
96% Alumina				
	0.010	0.005	142	203
	0.010	0.008	183	245
	0.010	0.010	203	264
	0.010	0.012	220	278
	0.015	0.005	112	166
	0.015	0.008	147	209
	0.015	0.010	166	229
	0.015	0.012	183	245
	0.025	0.005	81	125
	0.025	0.008	109	163
	0.025	0.010	125	183
	0.025	0.012	139	199
99.5% Alumina	0.010	0.005	151	210
	0.010	0.008	190	251
	0.010	0.010	210	269
	0.010	0.012	226	282
	0.015	0.005	122	175
	0.015	0.008	156	216
	0.015	0.010	175	235
	0.015	0.012	190	251
	0.025	0.005	93	135
	0.025	0.008	119	171
	0.025	0.010	135	190
	0.025	0.012	148	206

Beryllium Oxide at 25 °C	0.010	0.005	295	318
	0.010	0.008	310	334
	0.010	0.010	318	341
	0.010	0.012	324	346
	0.015	0.005	284	304
	0.015	0.008	297	320
	0.015	0.010	304	328
	0.015	0.012	310	334
	0.025	0.005	273	289
	0.025	0.008	283	303
	0.025	0.010	289	310
	0.025	0.012	294	317

Fabrication and its Effects on Thermal Management by *Guy W. Wagner* Thermal Management Concepts in Microelectronic Packaging
ISHM Technical Monograph 6984-003